

What is claimed is:

- 1 1. A method comprising:
2 invalidating an entry of a filter coupled to a
3 pipeline resource if an update to the entry occurs during a
4 context; and
5 flushing a portion of the pipeline resource
6 corresponding to an address space including the entry.
- 1 2. The method of claim 1, further comprising
2 flushing the portion upon a switch from the context.
- 1 3. The method of claim 1, wherein the pipeline
2 resource comprises a translation lookaside buffer.
- 1 4. The method of claim 1, further comprising
2 comparing an address obtained from an external snoop to a
3 plurality of entries in the filter to determine if the
4 update has occurred.
- 1 5. The method of claim 1, further comprising
2 flushing the portion of the pipeline resource via
3 microcode.
- 1 6. A method comprising:

2 flushing a portion of entries of a pipeline resource
3 if one of the portion of entries is updated during a
4 context.

1 7. The method of claim 6, further comprising
2 selectively flushing the portion of entries upon a switch
3 from the context.

1 8. The method of claim 7, wherein the portion of
2 entries comprises an address space corresponding to the
3 context.

1 9. The method of claim 6, wherein the pipeline
2 resource comprises a translation lookaside buffer.

1 10. The method of claim 9, further comprising
2 invalidating entries of a filter coupled to the translation
3 lookaside buffer corresponding to the portion of entries.

1 11. A method comprising:
2 loading an entry into a pipeline resource of a
3 processor, the entry corresponding to a page table; and
4 selectively flushing the entry if the page table is
5 updated during a context.

1 12. The method of claim 11, further comprising
2 selectively flushing the entry upon a switch from the
3 context.

1 13. The method of claim 11, further comprising
2 invalidating a filter entry of a filter coupled to the
3 pipeline resource, the filter entry corresponding to the
4 entry.

1 14. A method comprising:
2 loading an entry into a pipeline resource of a
3 processor, the entry corresponding to a page table; and
4 selectively updating the entry in the pipeline
5 resource if the page table is updated during a context.

1 15. The method of claim 14, further comprising
2 invalidating at least one filter entry of a filter
3 associated with the pipeline resource.

1 16. The method of claim 14, further comprising
2 preserving the updated entry in the pipeline resource on a
3 context switch.

1 17. An apparatus comprising:
2 a pipeline resource having a plurality of address
3 spaces, each of the plurality of address spaces

4 corresponding to one of a plurality of contexts, the
5 plurality of address spaces selectively flushable.

1 18. The apparatus of claim 17, wherein the pipeline
2 resource comprises a translation lookaside buffer.

1 19. The apparatus of claim 17, further comprising a
2 filter coupled to the pipeline resource to select at least
3 one of the plurality of address spaces to be flushed.

1 20. The apparatus of claim 19, wherein the filter
2 comprises a content addressable memory.

1 21. A method comprising:
2 dynamically partitioning a filter of a pipeline
3 resource into a plurality of partitions, each of the
4 partitions corresponding to one of a plurality of address
5 spaces.

1 22. The method of claim 21, further comprising
2 sharing the pipeline resource among a plurality of
3 applications, each corresponding to one of the plurality of
4 address spaces.

1 23. The method of claim 22, wherein each of the
2 plurality of partitions includes a fixed portion and
3 wherein the filter further comprises a dynamic portion.

1 24. The method of claim 23, further comprising
2 allocating at least part of the dynamic portion to one of
3 the plurality of applications that has consumed the fixed
4 portion of one of the plurality of partitions.

1 25. An article comprising a machine-readable storage
2 medium containing instructions that if executed enable a
3 system to:

4 dynamically partition a filter of a pipeline resource
5 into a plurality of partitions, each of the partitions
6 corresponding to one of a plurality of address spaces.

1 26. The article of claim 25, further comprising
2 instructions that if executed enable the system to permit a
3 plurality of applications, each corresponding to one of the
4 plurality of address spaces, to share the pipeline
5 resource.

1 27. The article of claim 26, further comprising
2 instructions that if executed enable the system to allocate
3 at least part of a dynamic portion of the filter to one of

4 the plurality of applications that has consumed one of the
5 plurality of partitions.

1 28. A system comprising:
2 a first processor having a pipeline resource having a
3 plurality of address spaces, each of the plurality of
4 address spaces corresponding to one of a plurality of
5 contexts, the plurality of address spaces selectively
6 flushable; and
7 a dynamic random access memory coupled to the first
8 processor.

1 29. The system of claim 28, further comprising a
2 second processor coupled to the first processor.

1 30. The system of claim 29, further comprising a
2 filter coupled to the pipeline resource to snoop address
3 information from the second processor.